CLAIMS

1. A sense amplifier for reading the contents of a memory cell in a transponder in an RFID system comprising:

a first transistor for receiving a read current from the memory cell,

a second transistor arranged for mirroring the read current,

a capacitor arranged to integrate the mirrored read current and provide a first voltage,

means for resetting the capacitor after a time period,

a second voltage,

a comparator defining an output and first and second inputs, wherein the output is responsive to the relative voltage levels on the first and second inputs, the first input connected to the first voltage, and the second input connected to the second voltage, wherein the comparator output determines the content of the memory cell.

2. The sense amplifier of claim 1 wherein the second voltage is a voltage signal derived from reading the contents of a second memory cell.

3. The sense amplifier of claim 1 wherein the second voltage corresponds to a threshold defining the boundary between a logic one and zero read from the memory cell.

4. The sense amplifier of claim 1 further including hysteresis in the comparator input.

5. The sense amplifier of claim 1 further comprising:

a second two transistor circuit for receiving, scaling and mirroring a second read current from a second memory cell,

a second capacitor arranged to integrate the mirrored and scaled second read current and to provide a second voltage,

means for resetting the second integrating capacitor after the time period,

means for connecting the second voltage to the second input of the comparator.

6. The sense amplifier of claim 1 further comprising:

a second two transistor circuit for receiving and mirroring a second read current from a second memory cell,

means for scaling the read current from the memory cell,

a second capacitor arranged to integrate the mirrored and scaled second read current and to provide a second voltage,

means for resetting the second integrating capacitor after the time period,

means for connecting the second voltage to the second input of the comparator.

7. The sense amplifier of claim 1 further comprising:

a second two transistor circuit for receiving and mirroring a second read current from a memory cell arranged to output a low read current,

a second capacitor arranged to integrate the mirrored second read current and provide a second voltage,

a third two transistor circuit for receiving and mirroring a third read current from a memory cell arranged to output a high read current,

a third capacitor arranged to integrate the mirrored third read current and provide a third voltage,

means for resetting the second and the third integrating capacitors after the time period,

means for averaging the second and third voltages together and connecting the averaged voltage to the second input of the comparator.

8. The sense amplifier of claim 7 wherein the means for averaging the second and third voltages is means for connecting them together.

9. The sense amplifier of claim 1 where the time period is more than about one microsecond.

10. A method for reading the contents of a memory cell in a transponder in an RFID system comprising the steps of:

receiving and mirroring the read current from the memory cell,

integrating the mirrored current on a capacitor thereby providing a first voltage,

resetting the capacitor after a time period, and

comparing the first voltage to a second voltage, and providing an output therefrom, wherein the output determines the logic content of the memory cell.

11. The method of claim 9 wherein the second voltage is a voltage derived from reading the contents of a memory cell.

12. The method of claim 9 wherein the second voltage corresponds to a threshold defining the boundary between a logic one and logic zero read from the memory cell.

13. The method of claim 9 wherein the step of comparing including providing hysteresis with respect to the switching of the comparator.

14. The method of claim 9 further comprising the steps of:

receiving, scaling and mirroring a second read current from a second memory cell,

integrating the mirrored second read current on a second capacitor and providing a second voltage,

resetting the second integrating capacitor after the time period, and

connecting the second voltage to the second input on the comparator.

15. The method of claim 9 further comprising:

receiving and mirroring a second read current from a memory cell arranged to output a low read current,

integrating the mirrored second read current on a second capacitor and providing a second voltage,

receiving and mirroring a third read current from a memory cell arranged to output a high read current,

integrating the mirrored third read current on a third capacitor and providing a third voltage,

resetting the second and the third integrating capacitors after the time period,

averaging the second and third voltages together and connecting the averaged voltage to the second input of the comparator.

16. The method of claim 9 further comprising the step of setting the time period to be greater than about one microsecond.